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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/854,213	05/11/2001	Gianfranco Bilardi	YOR920010439US1	7908

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EXAMINER
BAKER, PAUL A

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 09/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/854,213	BILARDI ET AL.	
	Examiner	Art Unit	
	Paul A Baker	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim~~s~~ 1 ~~is~~ rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "latter said memory level" is used throughout claim 1, only one memory level is stated which is insufficient to establish a "former vs. latter" comparison. For the purpose of this office action, all usage of the term "latter" in claim 1 will be ignored.

Claim Rejections - 35 USC § 103

Claims ~~1,2~~ are rejected under 35 U.S.C. 103(a) as being unpatentable over Cox, US Patent 5,357,621.

In regards to claim 1, Cox discloses a memory structure having a plurality of memory levels (figure 1 elements 20), a forward and return path for interconnecting the memory levels and a processor, a method of transferring requests from the processor on the forward paths and responses to the requests on the return path to the processor (figure 1 elements A and C), the method comprising;

transmitting each request from the processor to each of the levels (figure 1 elements A and C);

if a request from a memory level of the levels is a read to the memory of the memory level, then transmitting a response to the read request on the return path;

if a request from a memory level of the memory levels is a write request to the memory of the memory level then returning a response on the return path;

if a request from a memory level of the memory levels is targeted to a higher memory level of the memory level, then transmitting response on the return path; and

if a request from a memory level of the memory levels is targeted to a lower memory level of the memory level, then transmitting one response from of the memory level on the return path. (column 7 lines 26 – 32)

Cox however does not explicitly disclose internal buffers within the memory level or the return of two responses (two from buffer on write, one from buffer and response on read, two from buffer when a higher memory level is accessed). Cox discloses a microprocessor contained within the memory level, microprocessors frequently buffer Input/Output data (in addition to the register that latches the Input/Output data pins) to reduce the likelihood of loosing data. Cox notes the need for echoing back results as well as satisfying current memory level requests in column 7 lines 24 –31. Cox's invention echoes back any return messages from higher memory levels; therefore any pending return information would be propagated back to the processor. This would include multiple (i.e. two) responses.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include buffers into the microprocessor for the

purpose of maintaining data integrity and to return two responses for the purpose echoing all responses back to the processor.

In regards to claim 2, Cox does not disclose the internal buffer containing a depth of three, however the choice of the depth of the buffer is at the discretion of the designer and is typically made small for input/output buffers due to limited memory space in small processors. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the buffer depth to three for the purpose of limiting the amount of memory used.

In regards to claim 3, Cox discloses a memory structure for receiving requests to and transmitting responses from a memory in the structure, respectively, the structure comprising:

an ordered set of memory levels (figure 1 elements 20), each memory level having a controller and memory unit (figure 1 elements 13, 15, 17), which unit is a portion of the memory (figure 1 memory blk 1 and 2);

a forward path for transmitting the requests to the memory levels, starting from lower memory and proceeding to higher levels (figure 1 element A);

and a return path for transmitting responses to the requests from higher levels to the lower levels, wherein each controller at each memory level transmits responses to the requests on the return path from each level to a buffer in the controller at a lower level in accordance with the following algorithm (figure 1 element C):

a. if a request at any one of the levels is a read to the one level, then transmitting a response to the latter request on the return path to a controller of a memory level which is lower than the one level,

b. if a request at any one of the levels is a write to the one level, then transmitting two responses from internal buffers of the controller of the one level, then transmitting a response from the controller of the one level on the return path to a controller of a memory level which is lower than the one level,

c. if a request at any one of the levels is targeted to a higher of the levels, then transmitting a response from the controller of the one level of the return path to a controller of a memory level is lower than the one level, and

d. if a request at any one of the levels is targeted to a lower level, then transmitting one response to a request from the controller of the one level of the return path to a controller of a memory level which is lower than the one level (in column 7 lines 26 – 32).

Cox however does not explicitly disclose internal buffers within the memory level, however Cox discloses a microprocessor contained within the memory level, it is well known the use of microprocessor memory for input/output buffers for the purpose of reducing the likelihood of loosing data.

Cox also does not explicitly disclose the return of two responses (two from buffer on write, one from buffer and response on read, two from buffer when a higher memory level is accessed) however Cox notes the need for echoing back results as well as satisfying current memory level requests in column 7 lines 24 –31. Cox's invention

echoes back any return messages from higher memory levels; therefore any pending return information would be propagated back to the processor. This would include multiple (i.e. two) responses.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include buffers into the microprocessor for the purpose of maintaining data integrity and to return two responses for the purpose echoing all responses back to the processor.

In regards to claim 4, Cox does not disclose the internal buffer containing a depth of three, however the choice of the depth of the buffer is at the discretion of the designer and is typically made small for input/output buffers due to limited memory space in small processors. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to set the buffer depth to three for the purpose of limiting the amount of memory used.

In regards to claim 5, Cox does not disclose the return path twice the bandwidth of the forward path, however requests are unique and propagate sequentially up the memory levels, however one request may generate multiple responses from multiple memory levels resulting in a potential bottleneck on the return path. It is well known in the art that in order to relieve bottlenecks the bandwidth must be increased either the datapath must be wider or the clock rate must be increased. The widening of the datapath is well known (a 32 bit microprocessor can access twice the data per time unit

than a 16 bit microprocessor) and increasing the clock speed is well known (a bus operating at 200 MHz transmits twice the data per time unit than a bus operating at 100 MHz). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the return path with twice the bandwidth of the forward path for the purpose of reducing the potential for bottlenecking.

In regards to claim 6, Cox discloses each of the memory units has internal logic for copying data between one of the memory units and a request as specified therein, and forwarding one modified request to controllers on the return path in figure 1 elements 13, 14, and 15.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Soderquist, US Patent 6,425,064, discloses multileveled memory for storing vectors.

Jasper, US Patent 6,109,929, discloses a means of stacking memory modules.

Holman, WIPO 9930240, discloses memory module controller located on memory modules.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A Baker whose telephone number is (703)305-3304. The examiner can normally be reached on M-F 8am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo can be reached on (703)308-4908. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7238 for regular communications and (703)746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

PB
September 17, 2002

DO HYUN YOO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100